REMARKS

Favorable consideration of this Application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-16 are pending in the present Application. Claims 1, 6, 7, and 10-12 have been amended. Support for the amendment of Claims 1 and 10-12 can be found at least on pages 34 – 46 and Figs. 11 and 14. No new matter has been added.

By way of summary, the Official Action presents the following issues: Claims 1, 3-7 and 9-16 stand rejected under 35 U.S.C. § 103 as being unpatentable over Robinett et al. (U.S. Publication No. 2002/0131443, hereinafter Robinett) in view of Okura et al. (U.S. Patent No. 5,297,139, hereinafter Okura) and Domon (U.S. Patent No. 6,813,282); Claim 2 stands rejected under 35 U.S.C. § 103 as being unpatentable over Robinett in view of Okura and Domon, and further in view of Baker (U.S. Patent No. 5,948,080); and, Claim 8 stands rejected under 35 U.S.C. § 103 as being unpatentable over Robinett in view of Okura and Domon, and further in view of Saito et al. (U.S. Patent No. 6,523,696, hereinafter Saito).

REJECTION UNDER 35 U.S.C. § 103

The Official Action has rejected Claims 1, 3-7 and 9-16 are rejected under 35 U.S.C. § 103 as being unpatentable over Robinett et al. (U.S. Publication No. 2002/0131443, hereinafter Robinett) in view of Okura et al. (U.S. Patent No. 5,297,139, hereinafter Okura) and Domon (U.S. Patent No. 6,813,282). The Official Action cites Robinettt as disclosing the Applicant's invention with the exception of a detector for detecting the amount of data stored in a storage section and networks having non-coincident bus cycles. The Official Action cites Okura as disclosing the claimed detector and Domon as disclosing networks having non-coincident bus cycles and states it would have been obvious to one of ordinary

skill in the art the time the invention was made to combine the teachings of the cited references to arrive at the Applicant's claims. Applicant respectfully traverses the rejection.

Amended Claim 1 recites, *inter alia*, a data transfer apparatus, including:

> detection means for detecting the degree of non-coincidence between said first and second network and amount of data stored in said storage means, for each data flow; and
> control means for controlling said data transferred to said second network in accordance with a detection result provided by said detection means.

Robinett describes a system and associated method of remultiplexing program-bearing data of an MPEG transport stream (TS). Primarily, the system is directed to MPEG-2 compliant transport streams which carry video programs.

More specifically, adapters (110) function as a specialized synchronous interface and include direct memory access (DMA) control circuits (116). The DMA control circuit transfers transport packet data of the MPEG stream and descriptor data between the host memory (120) and the cache (114). The DMA control circuit enables continuous allocation of the descriptors and transport packet storage locations to incoming transport packets as they are received, i.e., from successive time slots.[1] In operation, an MPEG transport stream is received at a remultiplexer node (100) at one of a plurality of adapters (110). Each adapter is connected to a bus (130), which includes a host memory (120).

By inputting a separate MPEG transport stream to a corresponding adaptor, the remultiplexer functions to integrate and re-time transport packets to produce an output remultiplexed bit stream in accordance with MPEG decoding standards.

Okura describes a data communication system for decreasing transmission delay. The system includes nodes (110) having a multiplexed transmission line (6) including data

[1] Robinett at paragraph 76.

structured in a plurality of time slots (7). A transmission line access section (5) provides packet data (8) to a receiving buffer (2). The quantity of data written and accumulated in the buffer is compared with a predetermined threshold for a predetermined period from a read-start point of time. When the quantity of accumulated data is the same as or less than the predetermined threshold, the buffer performs only writing of data from the communication transmission line. When the quantity of accumulated data is larger than the predetermined threshold, the buffer performs both a read and write operation with respect to the buffer at the same time during a predetermined period.[2]

Domon describes a packet transfer device for bridging multiple IEEE 1394 networks. As shown in Fig. 1, input bus (40) and output bus (41) are connected by a bridge device (100). In operation, an isochronous packet is delayed with respect to input bus (40) in accordance with delay information (109) and then transmitted to bus (41). The delay is calculated by identifying the cycles (101) and (102) of the corresponding buses in cooperation with reference cycle identification information to account for differences in the cycle time of the IEEE 1394 data of the input side and that of the output side. Cycle time identifies to the portion of the 1394 cycle in which isonchronous data transfer is permitted.

In an operation of the present invention, the data transfer apparatus (42-2) may receive digital video data transmitted from digital video cassette recorder (11-1) by way of serial network (12-1), asynchronous network (15-1) and asynchronous network (15-2). Upon receipt of such data from serial network (15-2), the data transfer apparatus (42-2) stores such data in intermediate buffers such that different data flows are stored in different buffers. Detection circuitry is provided for detecting the degree of non-coincidence between a first and second network and the amount of data stored in the memory for each data flow. Control

[2] Okura at column 4, lines 33-54.

circuitry manages the transfer of data to the second network in accordance with a detection result of the detection circuitry. In this way, timing differences in the data caused by the non-coincident bus cycles of the first and second network, as well as underflow and overflow conditions, can be accounted for to eliminate undesirable artifacts in the reproduced digital video.[3] **Note that the claimed non-coincidence of the bus cycles is independent of 1394 timing as described in the cited text of Domon.**

Neither Robinett, alone or in combination with Okura and Domon, disclose or suggest transferring data between a first network and a second network, the second network having a non-coincident bus cycle with respect to the first network, wherein a memory status is detected so that control circuitry can transfer data to the second network in accordance with the detection result to avoid timing anomalies caused by non-coincident bus cycles, as recited in amended Claim 1 or any claim depending therefrom. Likewise, as independent Claims 10 and 11 recite substantially the same limitations discussed above, these claims, as well as any claims depending therefrom, are allowable at least for the same reasons.

With regard to Claim 7, the Official Action states that Robinett discloses that during an interval, when a node transport packet may be replaced with a data bearing transport packet corresponds to the Applicant's claimed substantial middle point of a predetermined period. Applicant wishes to point out that the term "period," as recited in the claims, is used in relation to a predetermined amount of data, such as a data frame. For example, as shown in Fig. 14, steps 87 and 92 illustrate the concept of inserting or discarding an empty packet at the middle (3072/2) of a period of frames. Robinett does not disclose or suggest this more detailed aspect of the Applicant's claim.

[3] Application at page 26, second full paragraph, 2 paragraph bridging pages 33 and 34.

Accordingly, Applicant respectfully requests that the rejection of Claim 1, 3-7 and 9-11 under 35 U.S.C. § 103 be withdrawn.

The Official Action has rejected Claim 2 under 35 U.S.C. § 103 as being unpatentable over the combination of Robinett in view of Okura and Domon, and in further view of Baker. The Official Action states that Robinett and Okura disclose all the Applicant's claim limitations with the exception of an IEEE-1394 serial bus. The Official Action cites Baker as teaching this more detailed aspect of the Applicant's invention and states that it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references for arriving at the Applicant's claims.

Applicant respectfully traverses the rejection. As discussed above, Robinett, neither alone or in combination with Okura and/or Domon, disclose or suggest the Applicant's data transfer apparatus including transferring data between a first network and a second network, the second network having a non-coincident bus cycle with respect to the first network wherein a memory status is detected so that control circuitry can transfer data to the second network in accordance with the detection result to avoid timing anomalies caused by non-coincident bus cycles. Likewise, Baker does not remedy this deficiency, and therefore, none of the cited references, either alone or in combination, can properly be asserted as disclosing or suggesting Applicant's Claim 2, which includes the above distinguished limitations by virtue of its dependency. Therefore, the Official Action does not provide a *prima facie* case of obviousness with regard to this claim.

Accordingly, Applicant respectfully requests that the rejection of Claim 2 under 35 U.S.C. § 103 be withdrawn.

The Official Action has rejected Claim 8 under 35 U.S.C. § 103 as being unpatentable over the combination of Robinett, Okura and Domon, and in further view of Saito. The

Official Action states that Robinett and Okura disclose all of the Applicant's claim limitations with the exception of a first network connected to another first network, which is not synchronous in terms of a network clock. The Official Action cites Saito as teaching this more detailed aspect of the Applicant's invention and states that it would have been obvious to one skilled in the art at the time the invention was made to combine the cited references for arriving at the Applicant's claims. Applicant respectfully traverses the rejection.

As discussed above, Robinett, neither alone or in combination with Okura and/or Domon, disclose or suggest the Applicant's data transfer apparatus, which includes transferring data between a first network and a second network, the second network having a non-coincident bus cycle with respect to the first network wherein a memory status is detected so that control circuitry can transfer data to the second network in accordance with the detection result to avoid timing anomalies caused by non-coincident bus cycles. Likewise, Saito does not remedy this deficiency; and. therefore, none of the cited references, either alone or in combination, can properly be asserted as disclosing or suggesting Applicant's Claim 8, which includes the above distinguished limitation by virtue of its dependency. Therefore, the Official Action does not provide a *prime facie* case of obviousness with regard to this claim.

Accordingly, Applicant respectfully requests that the rejection of Claim 8 under 35 U.S.C. § 103 be withdrawn.

CONCLUSION

Should the above distinctions be found unpersuasive, Applicants respectfully request that the Examiner provide an explanation via Advisory Action pursuant to MPEP § 714.13 specifically rebutting the points raised herein for purposes of facilitating the appeal process.

Consequently, in view of the foregoing Amendment and remarks, it is respectfully submitted that the present Application, including Claims 1-16, is patently distinguished over the prior art, in condition for allowance, and such action is respectfully requested at an early date.

Respectfully submitted,

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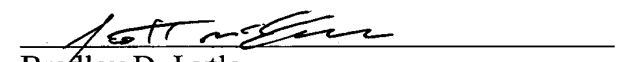

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